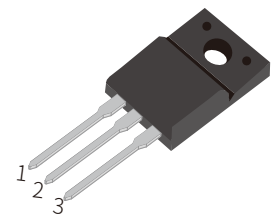


FEATURES

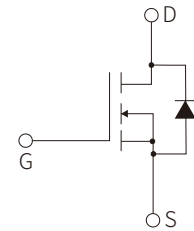
- | Low Gate Charge
- | Low ON Resistance
- | Improved dv/dt Capability
- | 100% Avalanche Tested



TO-220F

APPLICATION

- | Switching Mode Power Supplies (SMPS)
- | PWM Motor Controls
- | AC to DC Converters
- | LED Lighting
- | Adapter



Schematic Symbol

APPROVALS

RoHS	Compliance with 2011/65/EU
HF	Compliance with IEC61249-2-21:2003

ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	650	V
Continuous Drain Current	$T_c=25^{\circ}\text{C}$	I_D	12 ⁽¹⁾	A
	$T_c=100^{\circ}\text{C}$		7.5 ⁽¹⁾	A
Drain current pulsed ⁽²⁾		I_{DM}	40 ⁽¹⁾	A
Gate-Source Voltage		V_{GS}	± 30	V
Single pulsed Avalanche Energy ⁽³⁾		E_{AS}	576	mJ
Peak diode Recovery dv/dt ⁽⁴⁾		dv/dt	5	V/ns
Total power dissipation (@ $T_c=25^{\circ}\text{C}$)		P_D	24	W
Derating Factor above 25°C		P_D	0.19	W/°C
Operating Junction Temperature & Storage Temperature		T_{STG}, T_J	-55 to +150	°C
Maximum lead temperature for soldering purpose		T_L	260	°C
Thermal resistance, Junction to case (Maximum)		R_{thjc}	5.1	°C/W
Thermal resistance, Junction to ambient (Maximum)		R_{thja}	62	°C/W

Notes

1. Drain current is limited by maximum junction temperature.
3. $L = 12\text{mH}$, $I_{AS} = 3\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting at $T_J = 25^{\circ}\text{C}$

2. Repetitive rating : pulse width limited by junction temperature.
4. $I_{SD} \leq I_D$, $di/dt = 100\text{A/us}$, $V_{DD} \leq BV_{DSS}$, Starting at $T_J = 25^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (T_A=25°C)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain-source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	650			V
Breakdown voltage temperature coefficient	ΔBV _{DSS} / ΔT _J	I _D =250uA, referenced to 25°C		0.65		V/°C
Zero Gate Voltage Drain current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			1	uA
		V _{DS} =520V, T _C =125°C			50	uA
Gate Leakage Current	I _{GSS}	V _{GS} =30V ,V _{DS} =0V			100	nA
		V _{GS} =-30V ,V _{DS} =0V			-100	nA
Off Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	3.5	4.5	V
Drain-Source On-Resistance (note2)	R _{DS(on)}	V _{GS} =10V, I _D =2A		0.65	0.8	Ω
Forward Tran conductance	gFS	V _{DS} =10V, I _D =2A		9.6		S
Dynamic Characteristics						
Input capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f=1MHz		1890		pF
Output capacitance	C _{OSS}			144		pF
Reverse Transfer capacitance	C _{rss}			9.9		pF
Turn-on Delay Time	td(on)	V _{DS} =325V,I _D =4A, R _G =25Ω V _{GS} =10V		33		ns
Rising time	tf			41		ns
Turn-off Delay Time	td(off)			102		ns
Input capacitance	tf			37		ns
Total gate charge	Q _g	V _{DS} =325V,I _D =4A,V _{GS} =10V		38		nC
Gate-source charge	Q _{gs}			9		nC
Gate-drain charge	Q _{gd}			13		nC
Gate Resistance	R _g	V _{DS} =0V,Scan F mode		1.4		Ω
Continuous source current	I _S	Integral reverse p-n Junction diode in the MOSFET			12	A
Pulsed source current	I _{SM}				48	A
Diode forward voltage drop.	V _{SD}	I _S =4A, V _{GS} =0V			1.3	V
Reverse recovery time	Trr	I _S =4A, V _{GS} =0V, dI _F /dt=100A/us		480		ns
Reverse recovery Charge	Qrr			4.5		uC
Peak Reverse Recovery Current	Irrm	I _S =7A, dI _F /dt=100A/us		18.5		A

CHARACTERISTIC CURVES

Fig.1 Output characteristics

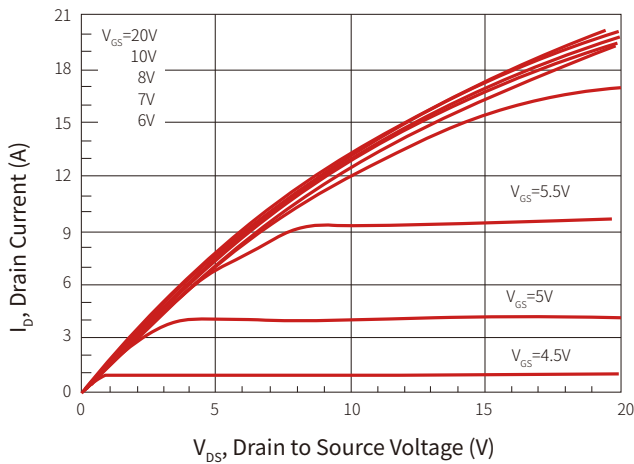


Fig.2 Reverse Characteristics

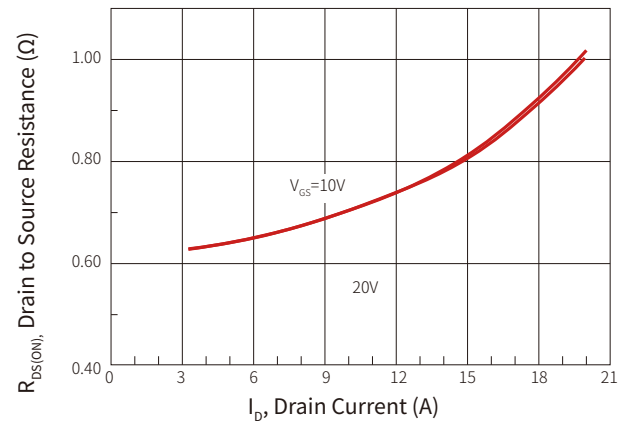


Fig.3 Gate charge characteristics

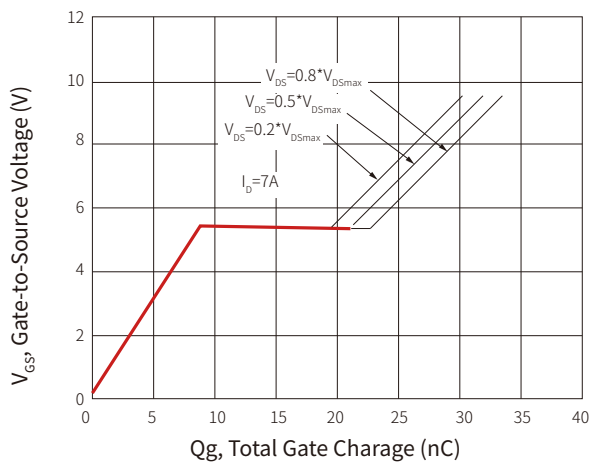


Fig.4 Capacitance Characteristics

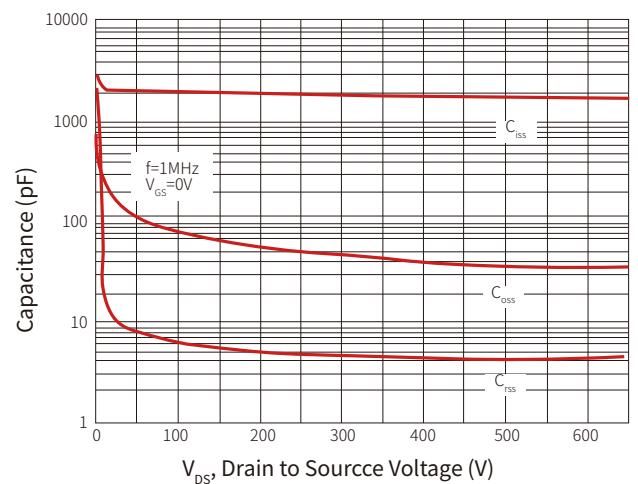


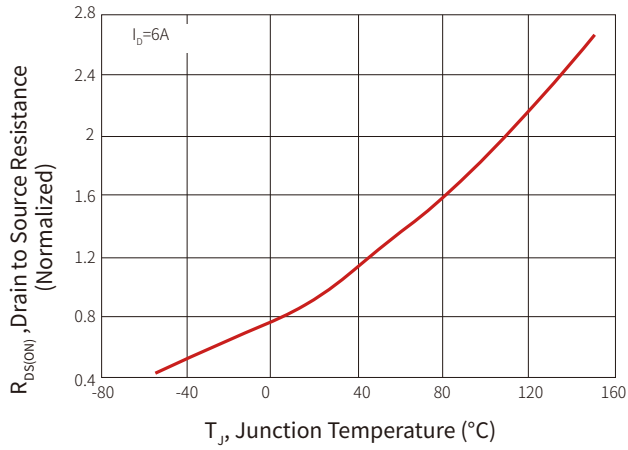
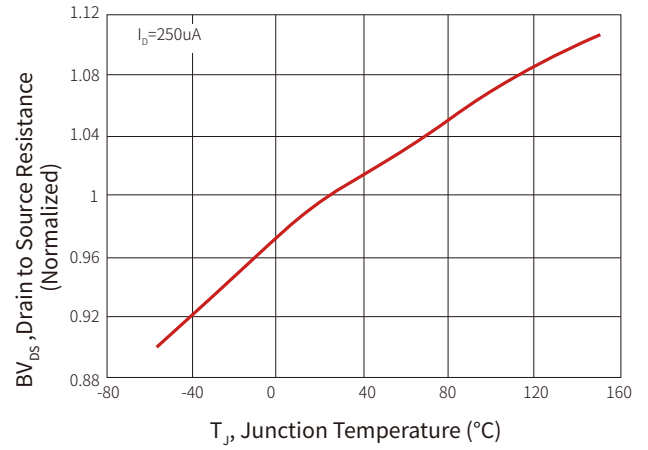
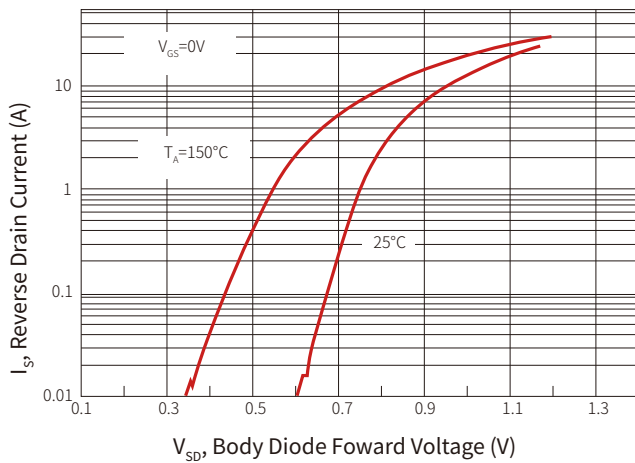
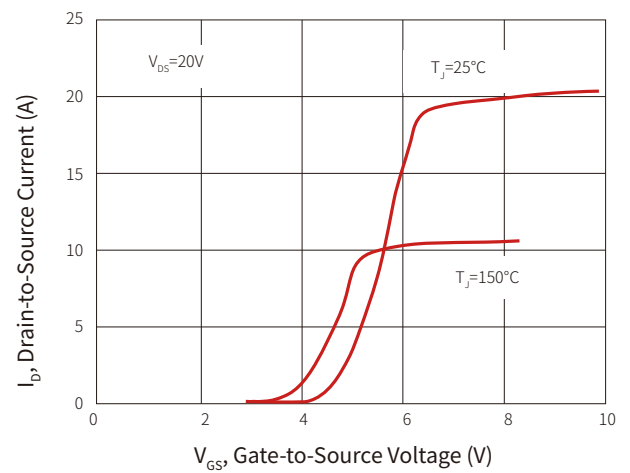
Fig.5 $R_{DS(ON)}$ vs junction temperature

Fig. 6 BV_{DSS} vs junction temperature

Fig.7 Forward characteristics of reverse diode

Fig.8 Transfer characteristics


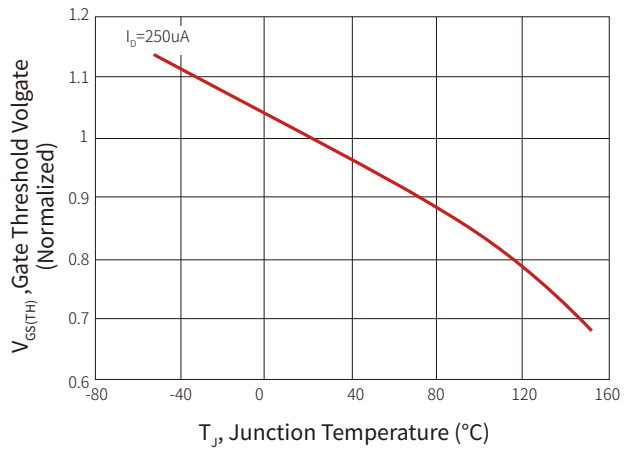
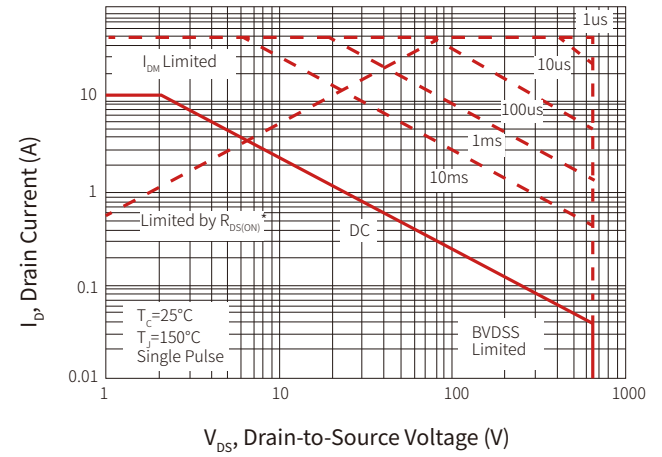
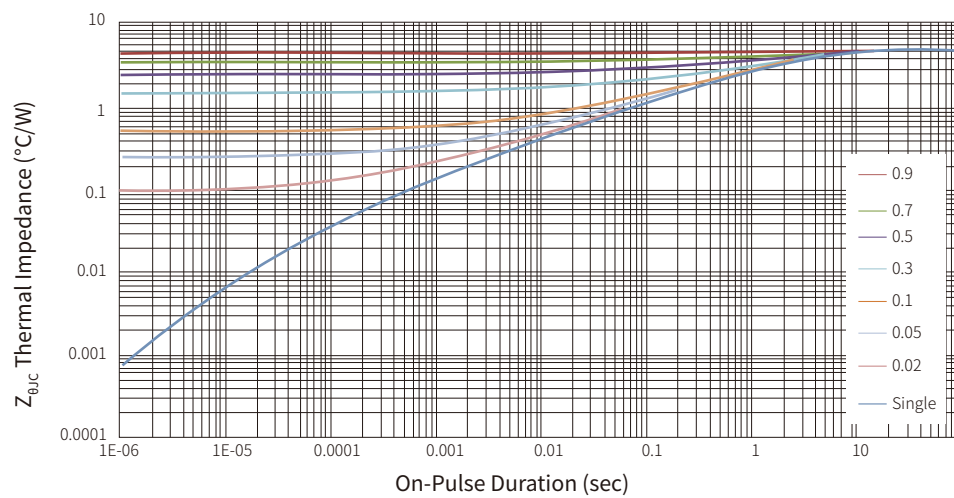
Fig.9 $V_{GS(TH)}$ vs junction temperature

Fig. 10 Safe operating area

Fig.11 Transient thermal impedance


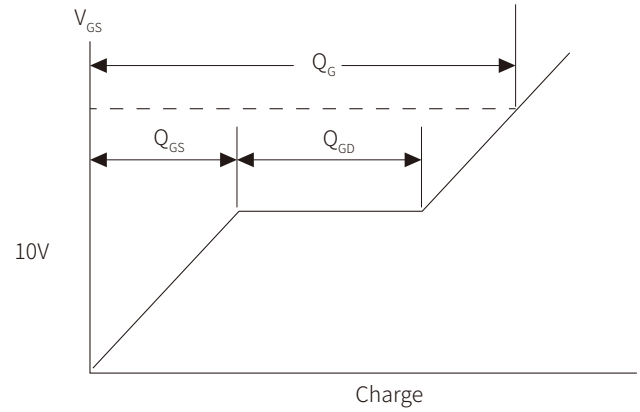
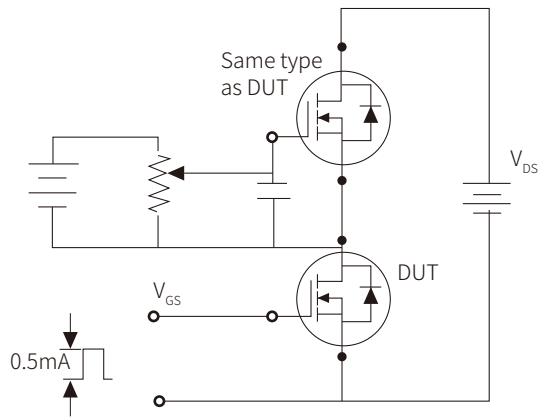
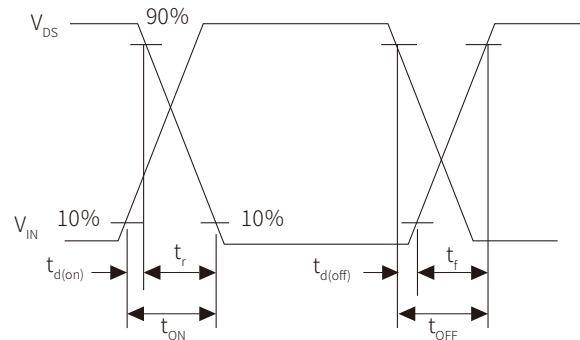
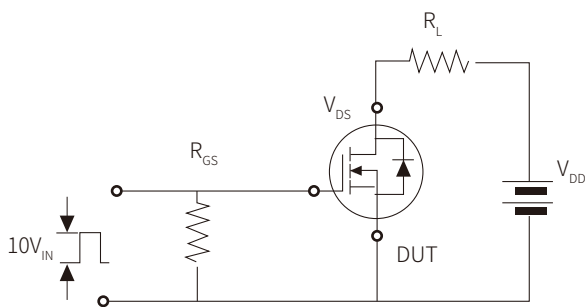
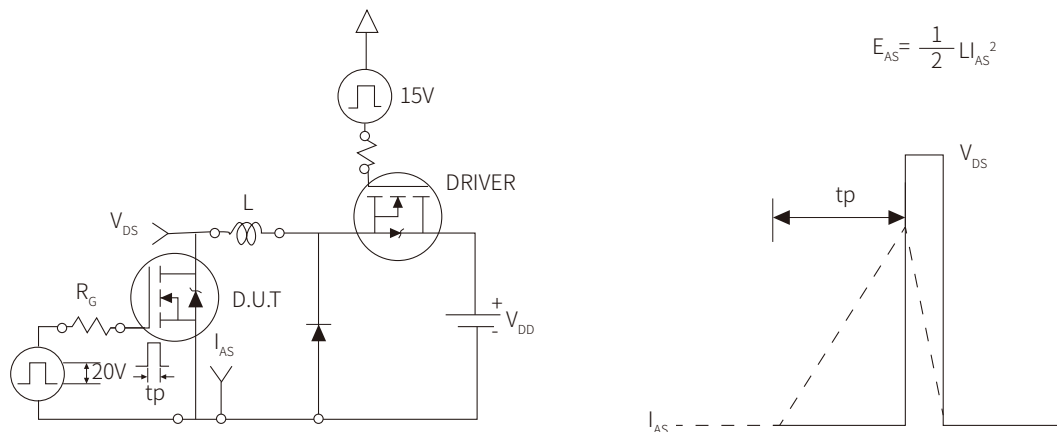
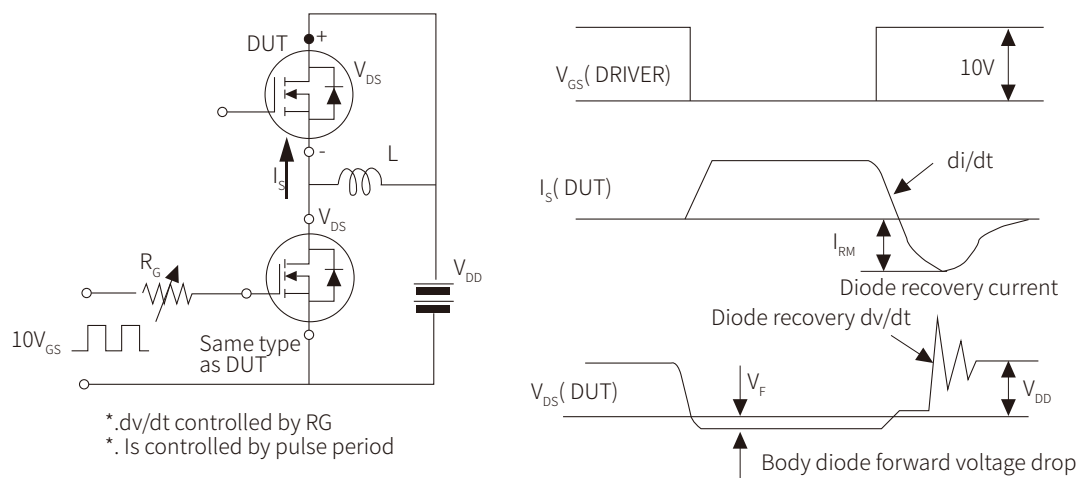
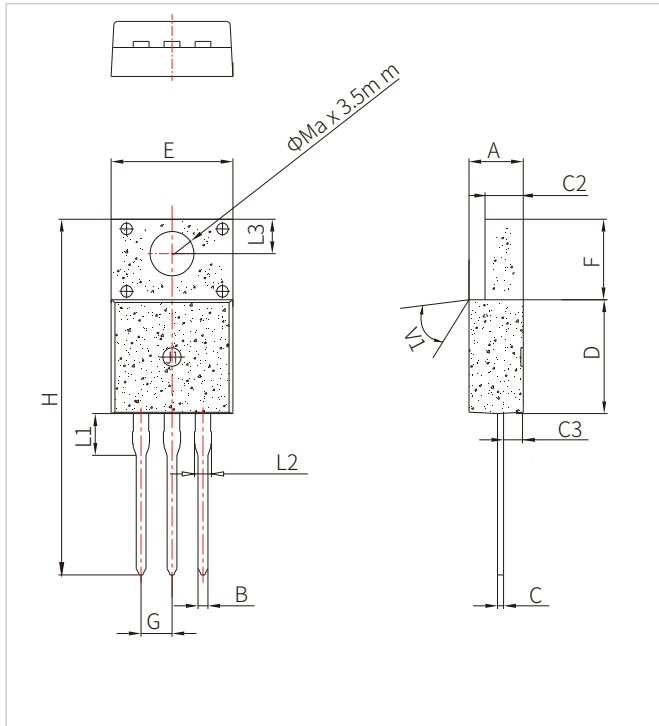
Fig.12 Gate charge test circuit & waveform

Fig.13 Switching time test circuit & waveform


Fig.14 Unclamped Inductive switching test circuit & waveform

Fig.15 Peak diode recovery dv/dt test circuit & waveform


TO-220F PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.90	0.173		0.193
B	0.74	0.80	0.83	0.029		0.033
C	0.45		0.75	0.018		0.030
C2	2.40		2.70	0.094		0.106
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.70		10.4	0.382		0.409
F	6.40		7.00	0.252		0.276
G		2.54			0.1	
H	28.0		30.0	1.102		1.181
L1		3.55			0.140	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	

ORDERING INFORMATION

Part Number	Component Package	Marking	QTY/Tube	Box
SNMF12N65	TO-220F	PDI12N65P2	50PCS	1000PCS

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